A HIGH-SPEED MONOLITHIC GaAs 10/11 COUNTER*

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ABSTRACT

Dual-gate GaAs MESFET logic has been used to develop a monolithic variable-modulus (÷10/÷11) counter. The circuit incorporates a novel feedback design that will allow the counter to operate up to the maximum speed of its flip-flop components, which have demonstrated cutoff frequencies above 2.5 GHz. The full counter has operated to 1.6 GHz while mounted in a coplanar test fixture. Operation above 2 GHz is expected when a test fixture with reduced crosstalk is used.

Introduction

Digital GaAs IC technology has reached the stage where circuits useful for systems application are beginning to emerge from the laboratory. This paper describes a monolithic GaAs variable-modulus counter that is useful as a high-speed prescalar circuit for communication applications. The circuit divides the frequency of the input signal by 10 or 11, depending on the voltages applied to the mode-control inputs. The speed of the circuit is maximized by incorporating a novel feedback design that allows the counter to function at full flip-flop speed. Devices have been fabricated with buffered depletion-mode (normally-on) GaAs MESFET logic, and operation has been achieved over the frequency range from dc to 1.6 GHz. Ultimately, operation above 2 GHz is expected.

Circuit Design

The design of the 10/11 counter is based on the use of dual-gate FETs, which enable the realization of OR-NAND and AND-NOR two-level logic gates, as shown in Figure 1. These merged logic gates provide more flexibility in logic design than is available when only single-gate FETs are used, and this flexibility leads to significant reductions in total device count, circuit area, and power dissipation. The basic building block of the counter circuit is the master-slave flip flop shown in Figure 2. Only four of the merged logic gates are needed to implement this flip flop. As a result, its maximum settling time is four gate delays. In addition, the flip flop operates with a single-phase clock, thereby eliminating any need to generate complementary CK and $\overline{CK}$ signals at microwave frequencies.

The schematic of the 10/11-counter circuit is shown in Figure 3. The ÷10/÷11 functions are achieved with six master-slave flip flops, synchronized to the input (clock) signal, plus appropriate feedback and mode-control circuitry. The full 10/11 counter requires only 25 gates to implement. In comparison, a recently reported GaAs 10/11 counter, implemented with Schottky-diode FET logic, requires 37 gates.[1] The two-level OR-NAND and AND-NOR logic gates enable the use of a novel logic design that optimizes the speed of the counter. The feedback logic is merged into the master latch of the first flip flop (FF1); the most time-critical feedback signal is generated by a look-ahead circuit that

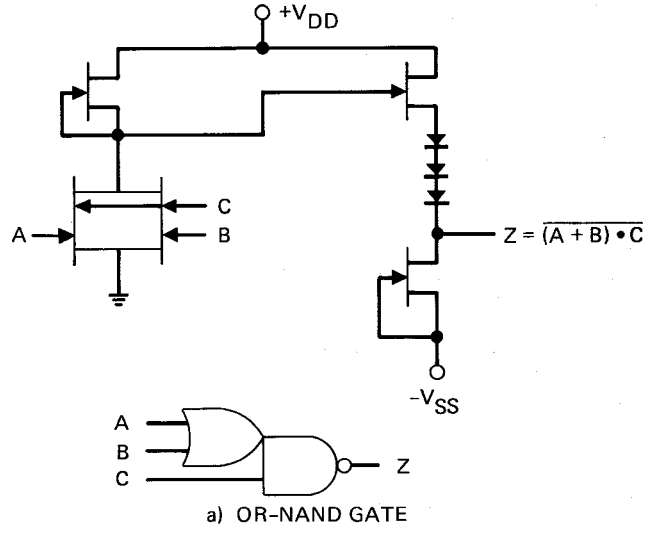

FIGURE 1. TWO-LEVEL LOGIC GATES IMPLEMENTED WITH DUAL-GATE FETs.

*This work was supported in part by the U.S. Army Electronics Research and Development Command under contract number DAAB07-78-C-2998.

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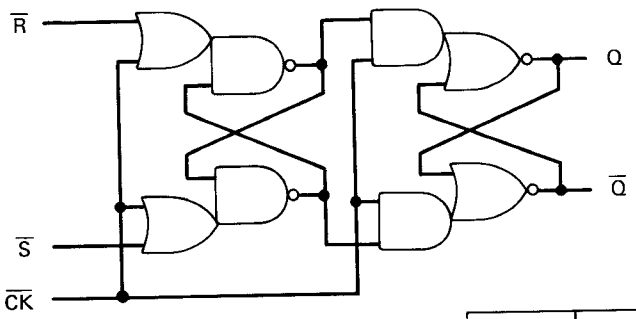

$\overline{S}_n$	$\overline{R}_n$	Q_{n+1}
0	0	?
0	1	1
1	0	0
1	1	Q_n

FIGURE 2. MASTER-SLAVE FLIP FLOP AND TRUTH TABLE.

operates in parallel with the slave latch of the sixth flip flop (FF6). Thus, the critical feedback signal is generated simultaneously with the state change of this flip flop. These techniques avoid the additional sequential time delays that normally result from the use of series feedback logic, and permit the counter to operate at speeds approaching the maximum toggle speed of the flip flops.

Two mode-control inputs are provided for user convenience. The mode-control logic is incorporated into the look-ahead circuitry. With one, or both mode-control inputs held high (logic 1), the counter acts as a five-stage recirculating shift register and divides the input frequency by ten. When both of the mode-control inputs are held low (logic 0), the length of the recirculation path alternates between five and six stages, providing divide-by-eleven operation. The counter logic is also self-clearing: it can be powered up in any arbitrary logic state and will automatically converge on the desired 10/11-counting sequence within 11 clock pulses.

Device Fabrication

Counter chips have been fabricated on n-type layers produced by direct implantation of Si^+ ions into Cr-doped semi-insulating GaAs substrates. Figure 4 shows a completed circuit. The chip measures 63 by 77 $mils^2$. In addition to the basic counter circuit, the chip includes buffer amplifiers for the input (clock) and output signals. Contact photolithography and lift-off technology are used throughout the fabrication process. Maximum FET speed is achieved by recessing the Schottky-barrier gates into the active channel layer; the depth of the channel etch is used to control the saturated drain current I_{DSS} and pinch-off voltage V_p of the devices. All the load FETs are 10-μm wide and their measured I_{DSS} is 2 mA. The widths of the devices in the output stages of the logic gates are optimized for gate speed as a function of fanout and interconnect capacitance using a technique similar to that of Barna and Liechti.[2] The lengths of the FET gates are 1.3 μm; the FET pinch-off voltages are nominally 1.5 V.

Circuit Performance

Figure 5 shows typical low-frequency (2 kHz) input and output waveforms experimentally obtained with the fabricated 10/11-counter circuits. The high and low logic levels are 0 V and -1.5 V, respectively. Typical dc bias supply voltages are V_{DD} = 3.6 V and V_{SS} = -2.5 V.

For testing at high speed, the chips were mounted on 1-in.-square alumina carriers containing 50-Ω coplanar transmission lines for input, output, and bias supply. The input signal was supplied by a cw signal generator. Correct 10/11-counter operation has been observed to 1.6 GHz with this setup (Figure 6). Although this performance is at the state of the art, we believe that the high-speed operation is currently limited by the test fixture, not the 10/11 counter. As seen in Figure 6, the use of coplanar circuits on the test board causes considerable rf coupling of the clock (input) signal into the dc bias and output lines. For example, at 1.6 GHz the clock signal in the output line has a peak-to-peak amplitude that is greater than the logic shift of the counter circuit. Coupling of the clock signal, especially into the dc-bias bus lines on the chip, degrades the high frequency performance of the counter. Use of an improved microwave test fixture that effectively isolates the input, output, and bias lines would substantially reduce the amount of rf noise appearing on the dc bus lines. The maximum speed of the counter should then approach the maximum toggle rate of its constituent flip flops. Test samples of the latter, which have been operated individually as binary dividers, have functioned correctly to frequencies above 2.5 GHz. The power dissipated by the counter is about 1.3 W at the lower frequencies, increasing to 2 W as the frequency increases from 1 to 1.6 GHz. Minor changes in the circuit design of the logic gates should reduce the dissipation to less than 1 W.

References

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2. A Barna and C. Liechti, "Optimization of GaAs MESFET Logic Gates with Subnanosecond Propagation Delays," IEEE J. Solid-State Circuit, SC-14, No. 4, August 1979.

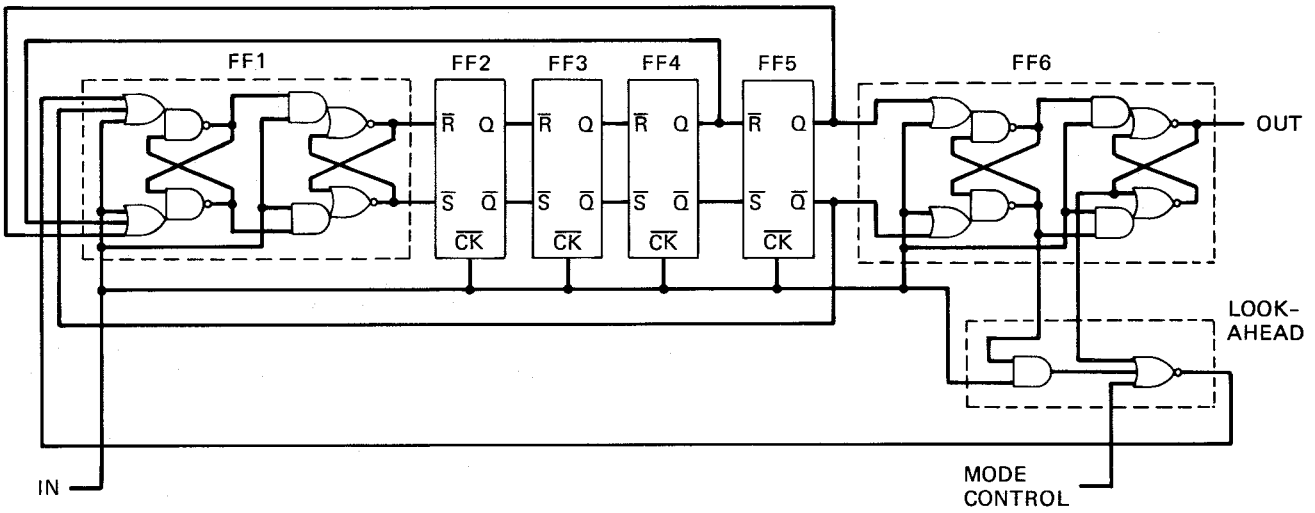

FIGURE 3. LOGIC SCHEMATIC OF 10/11 COUNTER.

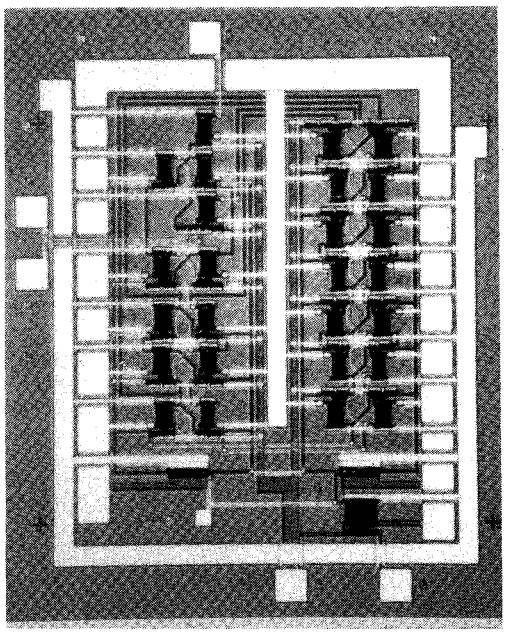

FIGURE 4. PHOTOMICROGRAPH OF PROGRAMMABLE 10/11 COUNTER CHIP.

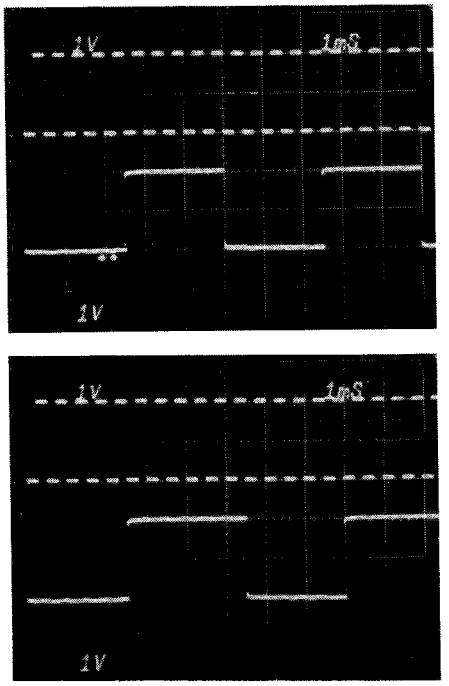

FIGURE 5. TYPICAL INPUT/OUTPUT SIGNALS FOR DIVIDE-BY-TEN (TOP) AND DIVIDE-BY-ELEVEN (BOTTOM) MODES AT LOW FREQUENCY (2 kHz).

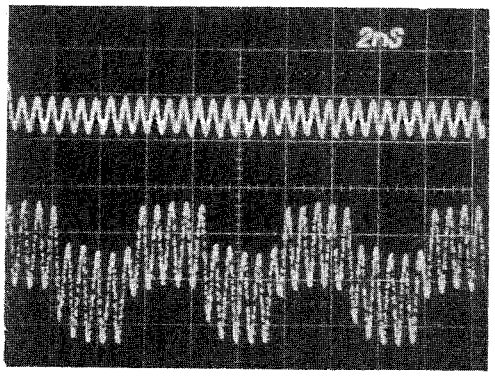

FIGURE 6. THE INPUT CLOCK SIGNAL (TOP) AND THE DIVIDE-BY-TEN OUTPUT (BOTTOM) AT 1.6 GHz. THE AMPLITUDES ARE NOT SHOWN TO SCALE.